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DESIGN OF HIGH FREQUENCY LOW POWER SWITCHED CAPACITOR FILTER FOR COMMUNICATION APPLICATION; A 10.7-MHz SIXTH-ORDER SC LADDER FILTER

N. BEHESHTI ROUY[1], R. NADERI ZARNAGHI[2] & J. SOBHI[3]

[1]Department of Electronics Engineering, Bostanabad Branch, Islamic Azad University, Bostanabad, Iran

[2]Department of Electronics Engineering, Heris Branch, Islamic Azad University, Heris, Iran

[3]Department of Electronic Engineering, University of Tabriz, Iran

ABSTRACT

In narrow-band high-speed switched-capacitor filters, the main limitation comes from the capacitance spread at the level and from amplifier settling time at the circuit level. In this paper most of the building blocks were used the regular clocks and the slower clocks are used in the filter termination only. The proposed telescopic amplifier with improved settling time performance has been prototyped in a 0.35 μm CMOS technology and characterized, experimental results have been presented. At last a sixth order band pass ladder switched-capacitor filter with a 400KHz bandwidth, center frequency of 10.7 MHz and main clock frequency of 47 MHz has been prototyped in a 0.35 μm CMOS technology. The filter is powered by the proposed telescopic amplifiers and uses a slower clock to reduce the capacitance spread as well. The power consumption of the whole chip is 37mWatts (including bias circuitry) and the power is 3.3v.

KEYWORDS: Capacitor Filter, Filter Design, Ladder Switched sc Filter, OTA Design

INTRODUCTION

Most of the high performance filters, sigma–data modulators and data converters are based on switched-capacitor (SC) techniques. Different architectures have been proposed in narrowband applications. In most of these operations, different methods are employed in order to optimize the operational transconductance amplifier (OTA), characteristics. For example two biquadrate filters connected in parallel running at 40 MHz each but acting in complementary clock phases lead to filters working at 80 Msamples/s [1,2]. BiCMOS gain-compensated single-stage OTAs and double-sampling techniques was used in Nagari's investigation. [3]. The main drawback of gain compensation techniques is that the precision depends on the feedback factor. hence, their application is difficult in complex structures.

N-path filter technique is proper for narrowband applications. In Chaderi, Quinn and Hartingsveldt investigations, this topology has been employed in high pass or Low pass first-order filters. [4,5,6] .Also, Although multistage amplifiers provide very large dc gain, usually these structures require capacitive compensation, which limits the system's frequency response [7]. One of the most popular topologies is called folded-cascade OTA. [12-14]. several optimization techniques are used. In Gray study, has been used gain-boosting technique that uses auxiliary amplifiers [9]. Design optimization and phase compensation schemes in Eynde and Nebel investigations [10,11] , multi-directions OTA in Tovmzou and olivera studies [12,13], AB Class based on OTAS in Roewer and castello techniques are unsuitable for low- voltage applications.

DESIGN CONSIDERATIONS FOR SWITCHED CAPACITOR FILTER

SC filters have simple structures with high quality. Now, they are considered as one of the successful techniques in the creation of analog filters in the integrated circuits. Cause to progress in CMOS operation amplifiers function and existence of high quality switches and capacitors, SC networks are widely used in analog sampled-data filters structure.

The aim of this paper is designing a SC filter integrated circuit used in communicative facilities. In this manner

power consumption should be small. In high frequency SC circuits power consumption is controlled by Op-Amp. Since, the accuracy of these filters change according to manufacturing physical parameters, finding low sensitive SC filter is important. SC filters consist of capacitors, analog switches and operation amplifiers. As compared with active–RC filters, these filters have many advantages. Under the same condition, location of filters pole is determined by capacitors ratio, RC product doesn't interfere in determination of poles location. Since capacitor ratio is controlled accurately for such filters and they are stable against temperature changes, a more accurate transfer function can be considered. Although, there is a main difference between active–RC and switched-capacitor filters, but SC filters belong to sampled- data analog filter category. So, in limited ranges of frequency spectrum, SC filters performance is proportionately equivalent to continuous time circuits (like active-RC filters) that input signal bandwidth is lower than switch frequency. It is recommended to use analysis of SC filters, sampled–data techniques and Laplace transform and Z tran form theory.

PROPOSED METHOD

In SC filter design, designing of a low power consumption and proper gain OTA is considered. In this case, telescopic OTA is proposed that uses gain boosting technique .

OTA Design

In this Study, sixth-order ladder filter was employed [1]. In figure 1 the main Op-Amp structural design is expressed. Auxiliary Op-Amp "A" is exactly the same as folded cascade Op-Amp shown in figure 2, that its inputs are pmos transitors. m_1,m_2 drain nodes are easily biased in low voltages.

Output resistance can be expressed as:

$$R_{out} = r_{up} \parallel r_{down} = [g_{m5} r_{o5} r_{o7}] \parallel [A.g_{m3} r_{o3} r_{o1}] \quad (1)$$

Where r_{up} is the equivalent resistance of upper transistors and r_{down} is the equivalent resistance of down transistors. Voltage gain is:

$$A_v = R_{out}.g_{ml} \quad (2)$$

where g_m is the transconductance of M_1

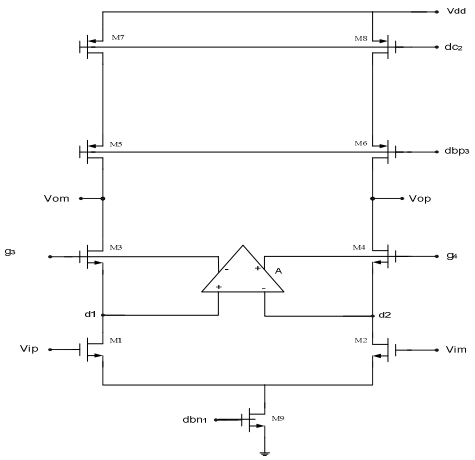

Figure 1: Main Op-Amp Structural Design

Auxiliary Op-Amp "A" was used in order to achieve lower power consumption without high drop in gain. In order to power acceleration, m1, m_2 transistors sizes are selected high so their output resistance is low.

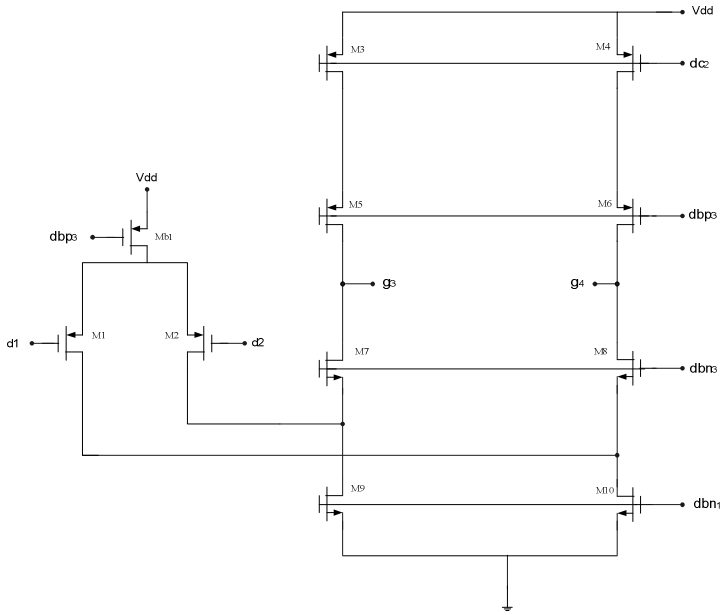

Figure 2: Auxilirary Op-Amp Structural Design

Thus, according to the R_{out} relation in telescopic Op-Amp

$$R_{out} = r_{up} \parallel r_{down} = [g_{m5} r_{o5} r_{o7}] \parallel [g_{m3} r_{o3} r_{o1}] \quad (3)$$

r_{up} is higher than r_{down} , so r_{down} reduces more output resistance. By adding auxiliary opamp A, r_{down} is increased equals to auxiliary op–amp gain and it increases output resistance.

Since upper transistors (m_5,m_7) are not in signal direction thus by increasing their length , their resistance enhanced, without defecting frequency response.

Filter Design

Figure 3 Shows SC filter circuit, this filter possess characteristics like BW= 400 KHz, f_0 = 10/7MHz and clock frequency equal 47 MHz. Resonance frequency is determined by the capacitors $[\theta \cong \frac{2\pi fo}{f_s}]\theta C$.

Using slower clocks allows reducing capacitive ratio without increase filter sensitivity. Equivalent resistance for SC state, that is created by periodic clocks, approximately follows $\frac{T}{C}\left[\frac{1}{f_s c}\right]$.

On which a signal is sampled in each K period, equivalent resistance increases by factor K too. Main idea for this state is shown in figure 4 for k=4. Φ_{11} and Φ_{22} are clock phases frequency which equals $\frac{f_s}{4}$ [1,16].

This design leads to lower capacitive ratio accompanied by reducing filter crisis parameters sensitivity relative to circuit components changes. Table 1 summarizes, capacitive values while using Φ_{11}, Φ_{22} clocks (Figures 3, 4).

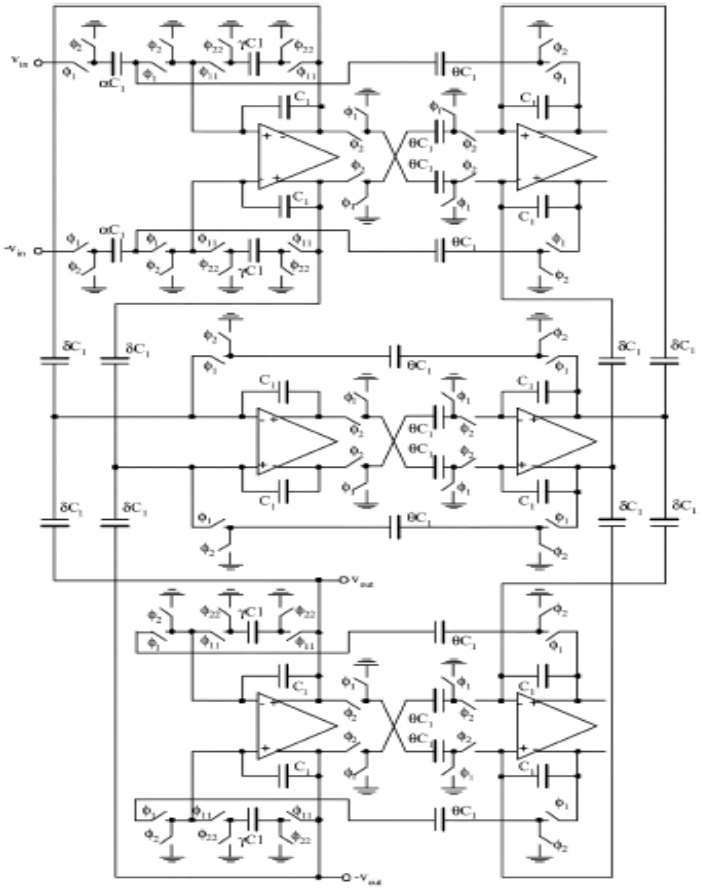

Figure 3: SC Filter Circuit

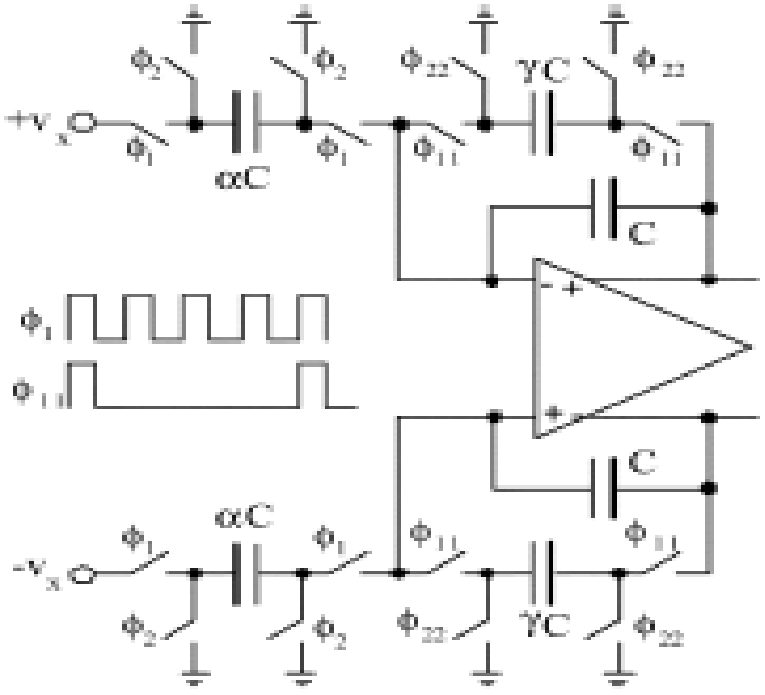

Figure 4: Equivalent Resistance Increases by Factor K

Table 1: Capacitive Values While Using Φ_{11}, Φ_{22} Clocks

Ratio	Secondary Clock (N=4)
δ=α	1/28
γ	1/28
θ	1
maximum spread	28

In this state required transmissibility for OTA reduced to g_m= 6.56 mA/V against g_m=9.3 mA/V required for primary design that slow clocks were not used. In this design, θ was considered near unit value. γ, δ values were considered the same for $\frac{f_s}{f_0} \cong 6.28$. Input capacitors $\alpha C_1 (= \sigma C_1)$ are selected for proportional pick gain value.

When the first integrator in figure 3 is consider with input capacitors $\theta = 1$ and $\alpha = \gamma = 1.32$, feedback factor will be 0.5. The value of smallest capacitor was 230ff because of nose ($KT/C = 2 \times 10^{-8} V_{rms}^2$) issue.

In order to have settling accuracy better than 0.5% ,it should be have $\frac{\delta}{w_{eff}} < T_{linear-settling}$ equation in integration phase.

According to the results, OTA conductivity gain is in the range of 6/54 mA/V . In order to having settling error lower than 1%, closed loop gain ($= A_{V\text{-}DC} \times \beta$) should be higher than 45dB. So $A_{V\text{-}Dc}$ will be greater than 51dB. SR higher than $(I_{out,\max} > 2mA \; if C_L = 6.6pf) 0/3 V/ns$ is required too. Since the PM is optimized in closed loop procedure, so open loop PM can be lower than 45° .

SIMULATION

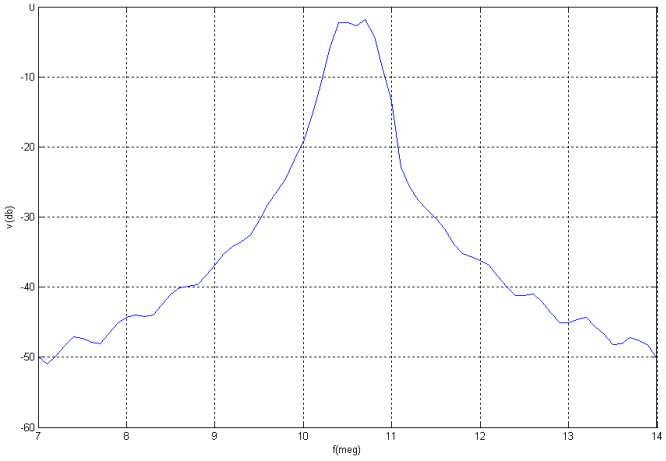

Figure 5: Filter Frequency Response-Hspice Result

The Six order Band pass filter with employed telescopic OTA, was simulated by Hspice software in 0.35 μm technology. The results will discuss latter.

Figure 5 shows filter frequency response with approximate bandwidth of 400 KHz and central frequency of 10.7MHz.

AC curve for OTA is shown in figure 6 illustrates gain equals 60db, PM=76.8 and approximate unit gain frequency is 1.17GHz.

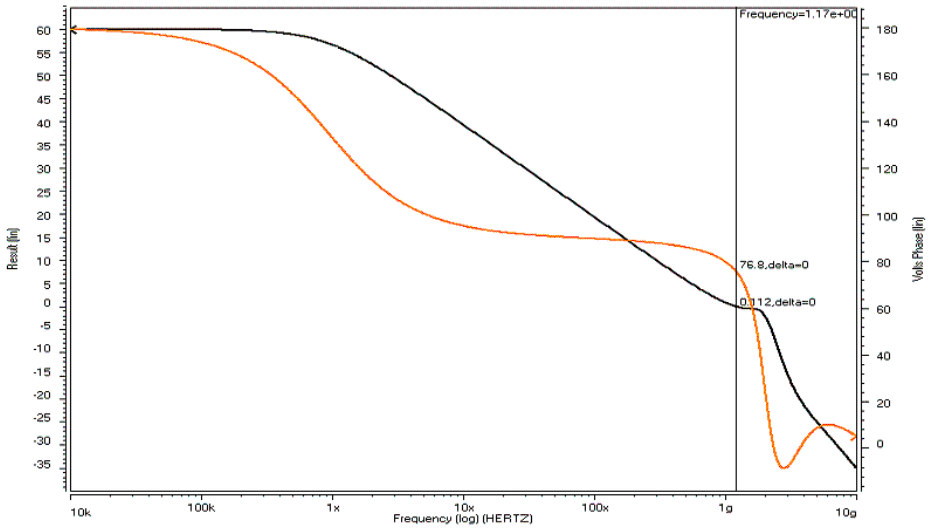

Figure 6: AC Curve for OTA-Hspice Result

Comparing filters designed for different intend such as power, level and sensitivity and etc. is difficult. Table 2 indicates experimental results of proposed circuit compared with other similar designs showing priority of our circuit.

Table 2: Experimental Results of Proposed Circuit Compared with Other Similar Designs

	Moon Study (9)	Cheung Study (26)	This Work
Tecnolgy[µm]	0.35µm CMOS	0.35µm CMOS	0.35µm CMOS
Filter type	Lp-ladder	2path biquads	Bp-ladder
Filter order	5	6	6
Fo[MHz]	12	44	10.7
BW[KHz]	1200	6280	400
Passband riple[db]	0.5	3	1
Q-section	1.5	1›	28
Attenuation at1.3fo	45›	25	45›
Supply voltage	5	3	3.3
Power-per-pol	25	15.5	6.7

CONCLUSIONS

In this paper a 10.7-MHz sixth-order SC ladder filter was designed. The filter is based on telescopic structure OTA by gain-boosting technique with enhanced SR. OTA settling – time is lower than 3.3 ns. Also the frequency of the slower clocks used equals $\frac{f_s}{4}$. Passband ripple is less than 1db throughout 400 KHz bandwidth. Total power consumption of filter is 37 mw, that it has reduced 30% relative to previous designs.

REFERENCES

1. J.Adult, J. Silva-Martinez, S. Member ,(2006). "A 10.7-MHz Sixth-Order SC Ladder Filter in 0.35 µm CMOS Technology" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, vol.53, pp.1625-1635

2. Patrick J,Quinn, Arthur H.M.,(2011). "Swithed-capacitor Techniques for High-Accuracy Filter and ADC Design" Springer, ISBN:1402062575

3. W.Sa-Nigiam vibool, B. Sriscuchinwong, (2007)."A 10.7-MHZ fully balanced, high-Q,107-dB-dynamic –range current-tunable bandpass filter" Journal of Science direct-Elsevier,vol.61,pp.307-313

4. M. B. Ghaderi, J. A. Nossek, and G. Temes,(1982)." Narrow-band switchedcapacitor bandpass filters" IEEE Trans. Circuits Syst., vol.18,no. 8, pp. 557–571

5. P. J. Quinn, (1998). "High-accuracy charge-redistribution SC video bandpass filter in standard CMOS" IEEE J. Solid-State Circuits, vol. 33, no. 7, pp. 963–975

6. P. J. Quinn, K. Hartingsveldt, and A. H. M. van Roermund,(2000). "A 10.7MHz CMOS SC radio IF filter using orthogonal hardware modulation" IEEE J. Solid-State Circuits, vol. 35, no. 12, pp.1865–1876

7. U. K. Moon, (2000). "CMOS high-frequency switched-capacitor filters for Telecommunication applications" IEEE J. Solid-State Circuits,vol.35 ,pp. 212–219

8. P. R. Gray and R. G. Meyer, (1982)." MOS operational amplifier design-A tutorial overview" ,IEEE J. Solid-State Circuits, vol. SC-17, no. 6 pp. 982-969

9. Bult and J. G. M. Geelen, (1990)."A fast-settling CMOS OpAmp for SC circuits with 90-dB dc gain" IEEE J. Solid-State Circuits, vol. 25, no. 6, pp.1379–1384

10. F. O. Eynde and W. Sansen,(1989). "Design and optimization of CMOS wide band amplifiers, in Proc." IEEE Custom Integr. Circuits Conf. (CICC'89), San Diego, May 1989, pp. 25.7.1–25.7.4.

11. G. Nebel, U. Kleine, and H. J. Pfleiderer,(1996). "Large bandwidth BiCMOS operational amplifers for SC video applications" IEEE J. Solid-State Circuits, vol. 31, no. 6, pp.828–834

12. C. Toumazou and S. Setty, (1998)."Feedforward compensation techniques for the design of low-voltage OPAMPs and OTAs," in Proc."IEEE Int. Symp. Circuits Syst. (ISCAS'98) , May 1998, vol. 1, pp. 367-464.

13. G. Olivera-Romero and J. Silva-Martinez,(1999). "A folded-cascode OTA based on complementary differential pairs for HF applications".Design of Mixed-Mode Integrated Circuits Design and Applications, pp. 57–60

14. F. Roewer and U. Kleine,(2002). "A novel class of complementary foldedcascode opamps for low-voltage" IEEE J. Solid-State Circuits, vol. 37,no. 8, pp.1080–1086

15. J. Ausin, J. Duque-Carrillo, G. Torelli,(2000)." Periodical nonuniform individually sampled switchedcapacitor circuits" IEEE Int. Symp. Circuits Syst. (ISCAS'00), pp. 449–452.